Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2757	vliw	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:35
L2	0	(control adj (engine unit logic)) with coprocessor with receive with instruction with (memory cache) with parallel	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:36
L3	252	712/24.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:36
L4	271	712/34.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:36
L5	131	vliw.ti.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:37
L7	40	(vliw "very long instruction word") same "branch unit"	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:38
L8	2	vliw with encryption	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:38
L9	0	vliw with atm	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:38
L10	0	viiw same encryption	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:39
L11	0	viiw and encryption	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:39
L12	5	vliw same ATM	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:39
L13	132	vliw and ATM	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:40
L14	0	"55485587".pn.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:40
L15	1	"5548587".pn.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:40
L16	15828	"asynchronous transfer mode"	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:41

L17	0	"asynchronous transfer mode" same viliw	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:42
L18	0	"asynchronous transfer mode" and viliw	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:42
L19	81	"asynchronous transfer mode" and vliw	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:42
L20	1	"asynchronous transfer mode" same vliw	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:42
L21	0	vliw and encrpyption	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:42
L22	258	vliw and encryption	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:43
L23	15	22 and 16	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:43
L24	7	16 and vliw and (AAL "ATM adaption layer")	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:46
L25	386205	direct$4 near3 connect$4	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:46
L26	9443	dedicated near3 (bus or connection)	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:47
L27	699	(25 or 26) with bidirectional	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:47
L28	97972	(main or program or instruction) adj (memory or storage or cache)	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:48
L29	6	27 with 28	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:48
L30	573996	microcontroller or controller or (control adj engine)	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:49
L31	5791	26 and 30	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:49
L32	802	26 with 30	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:50

L33	68660	dsp$1 or fpga$1 or coprocessor$1	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:50
L34	80	27 and 33	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:51
L35	9	27 and 32	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:54
L37	21978	control adj bus	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:55
L38	15527	30 and 37	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 14:55
L39	3169	33 and 38	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:03
L40	1488	28 and 39	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:04
L41	462	33 with 37	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:04
L42	364	30 and 41	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:05
L43	5	vliw and 42	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:13
L44	6	41 and simd	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:05
L45	1	("5450556").PN.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:28
L46	330	712/220.ccls.	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:28
L47	78	33 and 46	US-PGPUB; USPAT; EPO	OR	OFF	2005/09/10 15:28